U.S. Patent Application of

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relating to

TRACKING A CODE MODULATED SIGNAL

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TRACKING A CODE MODULATED SIGNAL

FIELD OF THE INVENTION

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The invention relates to a method, a processing unit, a system and a software program product, either supporting a correlation based tracking of a code modulated signal received at a receiver.

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BACKGROUND OF THE INVENTION

A tracking of received code modulated signals may be required, for example, in CDMA (Code Division Multiple

15 Access) spread spectrum communications.

For a spread spectrum communication in its basic form, a data sequence is used by a transmitting unit to modulate a sinusoidal carrier and then the bandwidth of the

20 resulting signal is spread to a much larger value. For spreading the bandwidth, the single-frequency carrier can be multiplied for example by a high-rate binary pseudo-random noise (PRN) code sequence comprising values of -1 and 1, which code sequence is known to a receiver. Thus,

25 the signal that is transmitted includes a data component, a PRN component, and a sinusoidal carrier component. A PRN code period comprises typically 1023 chips, the term chips being used to designate the bits of the code conveyed by the transmitted signal, as opposed to the

30 bits of the data sequence.

A well known system which is based on the evaluation of such code modulated signals is GPS (Global Positioning System). In GPS, code modulated signals are transmitted

1

by several satellites that orbit the earth and received by GPS receivers of which the current position is to be determined. Each of the satellites transmits two microwave carrier signals. One of these carrier signals

5   L1 is employed for carrying a navigation message and code signals of a standard positioning service (SPS). The L1 carrier signal is modulated by each satellite with a different C/A (Coarse Acquisition) Code known at the receivers. Thus, different channels are obtained for the

10   transmission by the different satellites. The C/A code, which is spreading the spectrum over a 1 MHz bandwidth, is repeated every 1023 chips, the epoch of the code being 1 ms. The carrier frequency of the L1 signal is further modulated with the navigation information at a bit rate

15   of 50 bit/s. The navigation information, which constitutes a data sequence, can be evaluated for example for determining the position of the respective receiver.

A receiver receiving a code modulated signal has to have

20   access to a synchronized replica of the employed modulation code, in order to be able to de-spread the data sequence of the signal. For de-spreading the data sequence, a synchronization has to be performed between the received code modulated signal and an available

25   replica code sequence. Usually, an initial synchronization called acquisition is employed for searching a satellite. Thereafter, a fine synchronization called tracking is employed for keeping the found satellite signal locked. In both synchronization

30   scenarios, a correlator is used to find the best match between the replica code sequence and the received signal and thus to find their relative shift called code phase.

A correlator aligns an incoming signal with a replica

2

code sequence with different assumptions on the code-phase. The correlator then multiplies the elements elementwise and integrates the resulting products to obtain a correlation value for each code-phase. If the

5   alignment is correct, the correlation will be higher than in the case of a misalignment. Thus, the correlation peak is an indication of the correct code-phase. The search by the correlator can be performed in addition with different assumptions on an additional frequency

10   modulation of the received signal.

Compared to the acquisition, the tracking searches in a smaller frequency range and code phase area. Still, the receiver usually comprises several tens of tracking

15   channels. Only simple operations are shared between the different channels when searching in parallel for several frequencies, for example for a compensation of sinusoidal modulation remaining after a carrier wipe-off. Therefore, also tracking correlators are rather complex.

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The tracking correlators of known receivers are implemented in hardware, and it is desirable to reduce the complexity of these correlators.

25   SUMMARY OF THE INVENTION

It is an object of the invention to reduce the complexity of parallel correlators which are employed for tracking acquired code modulated signals.

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It is further an object of the invention to reduce the computational load required in the tracking of acquired code modulated signals.

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A method is proposed for supporting a correlation based tracking of a code modulated signal received at a receiver. The samples of the received signal and of at least one available replica code sequence are aligned to
5   each other. Further, the positions of the samples in the received signal and in the at least one replica code sequence are grouped, each group comprising all positions at which the composition of the values of the samples of all of the at least one replica code sequence is similar.
10   The proposed method comprises as a first step combining the values of the samples of the received signal which are associated by their positions to a respective group separately for each group to obtain a respective intermediate result. As a second step, the proposed
15   method comprises determining a correlation value for each of the at least one replica code sequence by combining the intermediate results obtained for all groups separately for each of the at least one replica sequence, taking into account the values of the samples of the at
20   least one replica sequence in the respective group.

The receiver receiving the code modulated signal can be for example a part of a mobile terminal, and it can be for example inside the mobile terminal. This means that
25   the receiver can be for example a separate module or be implemented for example inside the mobile terminal. However, the receiver does not have to be combined with a mobile terminal. It can be for instance as well a normal GPS receiver which does not have a mobile terminal inside
30   the same device.

Further, a corresponding processing unit and a corresponding system are proposed, each comprising a first combining portion for generating the intermediate

4

results and a second combining portion for determining the correlation values in accordance with the proposed method.

5 The proposed processing unit can be for instance a tracking correlator, which may be included in a receiver or in some other apparatus which is adapted to receive from the receiver samples of the code modulated signal received at the receiver. Alternatively, the processing

10 unit can be given for example by the receiver itself or by some other apparatus which is adapted to receive from the receiver samples of the code modulated signal received at the receiver. The proposed system may comprise for example at least a receiver and an apparatus

15 which is adapted on the one hand to receive from the receiver samples of the code modulated signal and on the other hand to carry out the proposed method. Such an apparatus can be for instance a mobile terminal which comprises the receiver or which is connected to the

20 receiver or a network element of a mobile communication network which is able to communicate with such a mobile terminal.

Finally, a software program product is proposed, in which

25 a software code for supporting a correlation based tracking of a code modulated signal received at a receiver is stored, wherein samples of the received signal and samples of at least one available replica code sequence are aligned to each other and wherein positions

30 of the samples in the received signal and in the at least one replica code sequence are grouped, each group comprising all positions at which the composition of values of the samples of all of the at least one replica code sequence is similar. The software code realizes the

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steps of the proposed method when running in a processing unit.

The invention is based on the consideration that in each available replica code sequence checked in a tracking process, the same sample values will occur several times. In case of several replica code sequences, also a particular composition of sample values of all replica code sequences at one position will usually occur various times, if the number of replica code sequences is not too big and if the replica code sequence is a pseudorandom code sequence. It is therefore proposed that similar compositions of replica code sequence samples are grouped by the positions of the samples. The received samples are first combined within the groups, i.e. those received samples which are at positions associated to the same group are combined to form intermediate results. These intermediate results can be for example subsums obtained by accumulating the respective samples in an intermediate stage, but equally other calculation results. The intermediate results can then be combined to form a correlation value for each replica code sequence with a significantly reduced processing effort.

It is an advantage of the invention that it allows a savings in computations when processing in parallel several replica code sequences for tracking an acquired code modulated signal. The computations can be reduced for example to half, a third, or a fourth of the number of computations required for a conventional tracking. The invention can also be combined with known methods to save computations, for example when processing multiple frequencies. By such a combination, a significant reduction of the computational load can be achieved. As a

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result, also the power consumption is reduced.

It is further an advantage of the invention that the complexity of an employed tracking correlator can be

5   reduced by sharing the same hardware and intermediate results for processing several replica code sequences. This will reduce the gate count and the silicon area, which is of particular advantage for realizing a tracking in cellular phones and other mobile terminals.

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It is to be noted that the invention can be employed for a parallel processing of different replica code sequences, but equally for reducing the number of computations for the processing of a single replica code

15   sequence. In the latter case, the replica code sequence is partitioned into sections forming at least two different groups, i.e. each composition of samples comprises only a single sample. The calculation of the correlation value is then the same as for one of several

20   replica code sequences.

In case of a parallel processing, the invention can be employed for performing the tracking correlation in parallel for several replicas which correspond to the

25   code employed by several transmitting units, or in parallel for several code phases of a single replica which corresponds to the code employed by a single transmitting unit. The checked replica code sequences can thus originate from different replicas or from different

30   code phases of a single replica.

The positions of the samples can be grouped in different ways. In a first preferred approach, each group comprises all positions at which the composition of the values of

7

the samples of all replica code sequences is identical. In a second preferred approach, each group comprises all positions at which the composition of the differences between the values of the samples of all replica code
5   sequences except for one selected replica code sequence and the value of the sample of the selected replica code sequence is identical. When combining the intermediate results for obtaining the correlation value for a particular replica code sequence, the way in which the
10   groups are formed has to be taken into account.

The invention can moreover be employed with any type of code, since it is possible to form groups with similar replica samples for any code. A particularly simple
15   processing is obtained for binary codes, for example in the case of a BPSK (binary phase shift keying) modulation of the received signals, where the received samples and the samples of the replica code sequences have values of (-1,+1). In the latter case, each received sample has to
20   be multiplied either to +1 or -1 in the correlation process. With K replica code sequences, there are e.g. 2^K groups of replica samples with the same sign distribution for all replica code sequences at a specific sample position, or e.g. 2^{K-1} groups of replica samples with the
25   same distribution of sign changes compared to the sample of a selected one of the replica code sequences at a specific sample position. Since samples received for each of the groups are combined first within their groups, and the outputs of this operation are then combined
30   differently for each replica code sequence, several replica code sequences are processed with the computational effort of one.

The invention may be used in tracking for determining the

code phase and the frequency of a remaining complex sinusoidal modulation of a received signal, i.e. of the sinusoidal modulation which remains after the carrier has been wiped off from the received signal based on the

5 known nominal carrier frequency. The code phase is determined according to the peaks of a cross-correlation function, the correlation being calculated at initial code wipe-off stages. The processing for weak signals requires additional coherent and non-coherent

10 integrations. The invention can therefore also be used as a building block for other methods implementing different scenarios of coherent and/or non-coherent processing for possible multiple frequency candidates.

15 The invention can be implemented in hardware or in software. The invention can be implemented in particular in accordance with the implementation of the employed correlator.

20 The invention can further be employed in particular, though not exclusively, for CDMA spread spectrum receivers, for instance for a receiver of a positioning system like GPS or Galileo.

25 Other objects and features of the present invention will become apparent from the following detailed description considered in conjunction with the accompanying drawings. It is to be understood, however, that the drawings are designed solely for purposes of illustration and not as a

30 definition of the limits of the invention, for which reference should be made to the appended claims. It should be further understood that the drawings are not necessarily drawn to scale and that, unless otherwise indicated, they are merely intended to conceptually

illustrate the structures and procedures described
herein.

BRIEF DESCRIPTION OF THE FIGURES

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Fig. 1   presents a system in which the invention can be
          implemented;
Fig. 2   illustrates an exemplary distribution of sample
          values in three replica code sequences;
10   Fig. 3   is a diagram illustrating a first embodiment of
          the invention;
Fig. 4   is a flow chart illustrating the first embodiment
          of the invention;
Fig. 5   is a diagram illustrating a second embodiment of
15   the invention; and
Fig. 6   is a flow chart illustrating the second embodiment
          of the invention.

DETAILED DESCRIPTION OF THE INVENTION

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Two exemplary embodiments of the invention will be
described, which are implemented in a GPS receiver 11 of
a positioning system as presented in figure 1.

25   The system comprises a plurality of GPS satellites 16, a
mobile terminal 10 including the receiver 11, and a
mobile communication network 18. The receiver 11 includes
a receiving portion 12, a tracking portion 13 and a
memory 14.

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The memory 14 stores a plurality of replica code
sequences, each replica code sequence corresponding to
the code sequence employed by a respective GPS satellite
16. The GPS satellites 16 use BPSK (binary phase shift

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keying) PRN codes consisting of only +/-1. Therefore, also the stored replica code sequences are binary sequences. Alternatively, the replica samples could be generated in real-time. When a satellite signal, which

5   has previously been acquired by the receiver 11 in a known manner, reaches the receiver 11, the receiving portion 12 receives this satellite signal, wipes off the known carrier frequency from the received signal, and provides consecutive samples to the tracking portion 13.

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The tracking portion 13 employs a correlator 15 for calculating the correlation between the samples of a received signal and the available replica code sequences, to which the received samples are aligned. This process

15   is carried out for all to be searched code phases and will be explained in more detail below. The highest correlation value obtained identifies the satellite by which the received signal was transmitted and the code phase the received signal has. The code phases which are

20   to be searched are delimited by the preceding acquisition of the received signal. The correlator 15 can be implemented in software or in hardware.

The mobile terminal 10 comprising the GPS receiver 11 is

25   able to communicate with the mobile communication network 18. This may be exploited in a known manner to provide assistance data from the mobile communication network 18 to the GPS receiver 11, for instance for the acquisition of satellite signals. Alternatively or in addition, the

30   mobile terminal 10 may transmit information from the GPS receiver 11 to the mobile communication network 18 so that at least part of the processing described in the following could be carried out as well in the mobile communication network 18.

Figure 2 illustrates the alignment of received samples
and the samples of three replica sequences, which are
used for example in one integration cycle.

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A first row 20 presents samples of a received signal. A
second row 21 presents samples of a first replica code
sequence stored in the memory 14 of the receiver 11. A
third row 22 presents samples of a second replica code
10   sequence stored in the memory 14 of the receiver 11. A
fourth row 23 presents samples of a third replica code
sequence stored in the memory 14 of the receiver 11.
While the signs of the samples of a received signal
change in an unknown manner, the sign usage for each
15   sample of the stored replica code sequences is known to
the receiver.

The first embodiment of the invention will now be
described with reference to figures 3 and 4.

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Figure 3 illustrates the structure of a hardware-based
correlator 15 for the first embodiment of the invention.
The correlator 15 enables in the first embodiment a
parallel correlation based on three available replica
25   code sequences. Figure 4 is a flow chart illustrating a
corresponding parallel correlation either by software or
by hardware.

In the correlator 15 of figure 3, an input for input
30   samples is connected via a switch 31 and an adder 32 to a
demultiplexer 33. The demultiplexer 33 is connected via a
plurality of registers of a register bank 34 to a
multiplexer 35. The output of the multiplexer 35 is
provided on the one hand to a combiner 36 and coupled

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back on the other hand to a second input of the switch
31. The memory 14, which comprises at least these three
replica code sequences, is connected in parallel to a
control input of the demultiplexer 33 and to a control
5   input of the multiplexer 35.

The number of the registers of the register bank 34
corresponds to the number of possible compositions of
samples at the same position of the different replica
10   sequences. The signs of the replica samples at the same
position within the available replica code sequences are
coded for each possible composition as binary numbers,
where '0' stands for a negative sign while '1' indicates
a positive sign. An exemplary binary word of (01010)
15   would thus describe one possible composition of signs for
five replica code sequences, in which the samples of the
1st, 3rd and 5th sequence at a specific position are -1,
while the samples of the 2nd and 4th sequence at the same
specific position are +1. The more replica code sequences
20   are used, the more compositions are possible. If K
replicas are used, then the resulting binary words will
consist of K bits and the number of possible different
compositions are 2^K.

25   For the example of figure 3, which is based on three
available replica code sequences, there will be eight
possible compositions and thus eight different possibly
binary words:

30   (000), (001), (010), (011), (100), (101), (110), (111)

Consequently, the register bank 34 comprises eight
registers. Each of these registers can be addressed by a
respective one of the eight possible binary words.

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For performing the correlation, consecutive samples of
the received signal are provided by the receiving portion
12 as input samples to the correlator 15. For the current
5   correlator integration cycle, the samples of the input
signal are denoted as:

$$x_{N-1}, x_{N-2}, ..., x_3, x_2, x_1, x_0$$

10   where N is the number of samples.

At the same time, consecutive samples of replica code
sequences are provided by the memory 14 to the correlator
15. For the current correlator integration cycle, the
15   samples of the replica code sequences are denoted as:

$$r_{N-1}^k, r_{N-2}^k, ..., r_3^k, r_2^k, r_1^k, r_0^k$$

where N is again the number of samples and where $k = 1, ..., K$
20   identifies the respective replica code sequence. In the
example of figure 3, k is equal to 1, 2 or 3.

In a conventional tracking correlation, consecutive
samples of the received signal are multiplied to
25   consecutive samples of a known replica code sequence k,
and the resulting products are integrated for obtaining
correlation values c^k for the particular iteration and
thus the particular code phase according to the equation:

30   $$c^k = \sum_{j=0}^{N-1} r_j^k x_j$$

Compared to this conventional approach, the tracking

14

correlation according to the first embodiment of the invention results in the same correlation values C^k with a reduced amount of processing and thus a reduced complexity.

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Corresponding to the above identified 2^K possible binary words (000) to (111) for addressing the registers, 2^K groups of K samples with different "sign" usage are defined, which are denoted as $J_{b_1...b_K}$. $b_1...b_K$ is the notation of signs for a respective group. In the embodiment of

10 figure 3, there are thus eight groups J_{-1-1-1} to J_{+1+1+1}, each identifying another group of samples with a specific sign usage.

15 The position j is defined to belong to a specific one of the groups $J_{b_1...b_K}$, if the value of the samples at position j of the K replica code sequences correspond to the values of $b_1...b_K$ of this group, i.e. $j \in J_{b_1...b_K}$, if

$$\left(r_j^1 .. r_j^K \right) = \left(b_1,...,b_K \right).$$

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Now, subsums of samples S_m are calculated in each group according to the equation:

$$S_m = \sum_{j \in J_{b_1...b_K}} x_j \, ,$$

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where $m = \left(m_1,...,m_K \right) = 0,1,...,2^K - 1$ is reserved for indexing the groups $J_{b_1...b_K}$, with $m_p = \begin{cases} 1 & b_p = 1 \\ 0 & b_p = -1 \end{cases}$ and $p = 1...K$.

In the example of figure 3, the index m thus corresponds

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to a respective one of the above listed eight binary words (000) to (111) having the values 0 to 7. The index m thereby associates the respective subsum S_m to one of the eight different groups $J_{b_1...b_K}$.

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For calculating the subsum S_m for each group in a new integration cycle, the correlator 15 first initializes the value in each of the 2^K registers of the register bank 34 to zero. Each of the register values constitutes the
10   current value of one of the subsums S_m, the index m identifying the respective register. The initialization of the subsums S_m is indicated as step 401 of figure 4.

Then, the correlator 15 receives input samples x_j one
15   after the other for forming the final subsums S_m. The sample x_j is provided via the switch 31 to the adder 32. The samples of the three replica code sequences having the same index j are r_j^1, r_j^2 and r_j^3. These samples are used for controlling the demultiplexer 33 and the
20   multiplexer 35. The demultiplexer 33 and the multiplexer 35 are able to address a respective register of the register bank 34 by selecting a register address comprising a '0' for each negative sign and a '1' for each positive sign of the applied replica code samples
25   r_j^1, r_j^2 and r_j^3. For example, with $r_j^1 = -1$, $r_j^2 = +1$ and $r_j^3 = -1$, a register address (010) is selected. When the input sample x_j has been forwarded to the adder 32, the multiplexer 35 provides the current value of the subsum S_m in the register to which the currently selected register
30   address is associated via the switch 31 to the adder 32. With the assumed register address (010), this is the subsum $S_{(010)}$ or S_2. The adder 32 adds the value of the

16

current input sample x_j to the value of the retrieved subsum S_m. The new sum S_m is then stored again via the demultiplexer 33 into the register of the register bank 34 to which the selected register address is associated.

5   The calculation of the subsums S_m is indicated in figure 4 as step 402.

This procedure is performed for the current integration cycle analogously for all N input samples x_n.

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After a respective integration cycle, the multiplexer 35 outputs the value of the subsums S_m in all registers to the combining unit 36. The combining unit 36 combines all subsums S_m with the values within the different groups to

15   obtain the K correlation values C^k.

For the kth replica code sequence, with $k = 1,...,K$, the correlation value is determined according to the equation:

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$$C^k = \sum_{m=0}^{2^K-1} b_{k,m} S_m$$

where for a respective value of m with $m = (m_1,...,m_K)$, $b_{k,m}$ is

defined to be $b_{k,m} = \begin{cases} 1 & m_k = 1 \\ -1 & m_k = 0 \end{cases}$ for the kth replica code

25   sequence $k = 1,...,K$. Thus, the value of b_k depends on the replica code sequence k and on the group m for which it is needed in the sum.

In the example of figure 3, a dedicated correlation value

30   C^1, C^2, C^3 has to be calculated for $K=3$ replica code

sequences, and the number of groups is eight. The sum in the equation for calculating a respective correlation value thus runs from $m=0$ to $m=7$. In the third term of the sum, for instance, m is equal to 2 and corresponds as

5 binary word to $m=(m_1,m_2,m_3)=(010)$. For the first replica code sequence, k is equal to 1 and therefore $m_k=m_1=0$. As consequence, b_k is equal to -1. Thus, the third term of the sum for calculating the correlation value C^1 for the first replica code sequence is $b_kS_m=(-1)*S_2$. The other

10 terms of the sum are determined analogously for each of the replica code sequences.

The calculation of the correlation value C^k for each replica code sequence is indicated in figure 4 as step

15 403.

Components 31 to 35 thus form a first combining portion and the combining unit 36 a second combining portion. Each register of the register bank 34 forms part of

20 another intermediate accumulator in the first combining portion, which is used for performing a significant part of computations for all K replica code sequences at once.

The second embodiment of the invention will now be

25 described with reference to figures 5 and 6.

Figure 5 illustrates the structure of a hardware-based correlator 15 for the second embodiment of the invention. The correlator 15 enables in the second embodiment a

30 parallel correlation based on four available replica code sequences. Figure 6 is a flow chart illustrating a corresponding parallel correlation either by software or by hardware.

The structure of the correlator 15 for the second embodiment is similar to the structure depicted in figure 3. It comprises a switch 51, an adder 52, a demultiplexer

5   53, a register 54, a multiplexer 55 and a combining unit 56 which are arranged in the same manner as in figure 3.

In this case, however, the memory 14 of the receiver 11 comprises at least four replica code sequences. It is

10 connected for the first replica code sequence to the adder 52 and to a respective first input of three XOR gates of an XOR logic 57. The memory 14 is further connected for the second replica code sequence to the second input of the first XOR gate of the XOR logic 57,

15 for the third replica code sequence to the second input of the second XOR gate of the XOR logic 57 and for the third replica code sequence to the second input of the third XOR gate of the XOR logic 57. The outputs of the of the XOR logic 57 are applied in common to the control

20 input of the demultiplexer 53 and to the control input of the multiplexer 55.

For performing the correlation, consecutive samples of the received signal are provided by the receiving portion

25 12 as input samples to the correlator 15. For the current correlator integration cycle, the samples of the input signal are denoted again as:

$x_{N-1}, x_{N-2}, ..., x_3, x_2, x_1, x_0$

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where N is the number of samples.

At the same time, consecutive samples of replica code

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sequences are provided by the memory 14 to the correlator 15. For the current correlator integration cycle, the samples of the replica code sequences are denoted as:

5    $r_{N-1}^k, r_{N-2}^k, ..., r_3^k, r_2^k, r_1^k, r_0^k$

where N is again the number of samples and where $k = 0, ..., K$ identifies a respective replica code sequence, $k = 0$ being reserved for the first replica code sequence. In the
10   example of figure 5, K is equal to three.

The number of registers of the register bank corresponds to the number of possible compositions of sign changes when comparing a sample at a specific position of a first
15   replica signal to a sample at the same position of a respective one of the further replica signals. More specifically, the sign changes in the samples of the further replica code sequences are coded for each possible composition as binary numbers, where '0' stands
20   for no change of sign while '1' indicates a change of sign compared to the sample at the same position of the first replica code sequence. An exemplary binary word of (01010) would thus describe a possible composition of sign changes for six available replica code sequences, in
25   which the samples of the 2st, 4rd and 6th sequence at a specific position are equal to the sample of the 1st sequence at the same position, while the sampled of the 3nd and 5th sequence at this position are different from the sample of the 1st sequence at this position. The more
30   replica code sequences are used, the more compositions of sign changes are possible. If $K+1$ replica code sequences are used, then the binary words will consist of K bits and the number of possible different compositions are 2^K.

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For the example of figure 5, which is based on four available replica code sequences, there will be eight possible compositions of sign changes and thus eight different possible binary words:

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(000), (001), (010), (011), (100), (101), (110), (111)

Thus, the register bank comprises eight registers. Each of these registers can be addressed by another one of the
10   eight possible binary words.

As mentioned above, in a conventional tracking correlation, the correlation values c^k are calculated according to the equation:

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$$C^k = \sum_{j=0}^{N-1} r_j^k x_j$$

Also in the tracking correlation according to the second embodiment of the invention, the amount of processing
20   required for obtaining the correlation values c^k is reduced without approximations.

Corresponding to the above identified 2^K possible binary words (000) to (111) for addressing the registers, 2^K
25   groups of K samples with different "sign" changes are defined, which are denoted as $J_{b_1...b_K}$. $b_1...b_K$ is the notation of sign changes with respect to the first replica code sequence for a respective group, i.e. $b_p = \left(r_j^p \cdot r_j^0 \right)$ with $p=1...K$. In the second embodiment illustrated in figure 5,
30   there are thus eight groups J_{-1-1-1} to J_{+1+1+1}, each identifying a group of samples with similar sign change behavior.

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The position j is defined to belong to a specific one of the groups $J_{b_1...b_K}$, if the sign changes of the samples at position j of the K last replica code sequences compared to the sample at position j of the first replica code sequence correspond to the values of $b_1...b_K$ of this group, i.e. $j \in J_{b_1...b_K}$, if $\left(r_j^0 r_j^1 ... r_j^K \right) = \pm \left(1, b_1, ..., b_K \right)$.

Now, subsums S_m are calculated in each group according to the equation:

$$S_m = \sum_{j \in J_{b_1...b_K}} r_j^0 x_j$$

where $m = \left(m_1, ..., m_K \right) = 0,1,...,2^K - 1$ is reserved for indexing the groups $J_{b_1...b_K}$ with $m_p = \begin{cases} 1 & b_p = 1 \\ 0 & b_p = -1 \end{cases}$ and $p=1...K$.

Thus, in the example of figure 5, the index m corresponds to a respective one of the above listed eight binary words (000) to (111) having the values 0 to 7. The index m thereby associates the respective sum S_m to one of the eight different groups $J_{b_1...b_K}$.

For calculating the subsum S_m for each group for a new integration cycle, also the correlator 15 of the second embodiment first initializes the values in each of the 2^K registers to zero. Each of the register values constitutes the current value of one of the subsums S_m, the index m identifying the respective register. This is indicated as step 601 of figure 6.

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Then, the correlator 15 receives input samples x_j one after the other for forming the final subsums S_m. The respective sample x_j is provided via the switch 51 to the
5   adder 52. The samples of the four replica code sequences having the same index j are r_j^0, r_j^1, r_j^2 and r_j^3. The sample r_j^0 of the first replica code sequence is equally provided to the adder 52. Here, the input sample x_j is multiplied with the sample r_j^0 of the first replica code sequence at
10   the same position j.

Further, a register address is generated by combining the sample of the first replica code sequence separately with each of the samples of the further replica code sequence
15   at position j. In the example of figure 5, this is achieved by means of the XOR logic 57. The XOR logic 57 outputs a value '0' for each sample of the second to fourth replica code sequence at position j which is equal to the sample of the first replica code sequence at
20   position j and a '1' for each sample of the second to fourth replica code sequence at position j which is different from the sample of the first replica code sequence at position j. The samples of the four replica code sequences having the same index j may be for example
25   $r_j^0 = +1$, $r_j^1 = +1$, $r_j^2 = -1$, $r_j^3 = +1$. These samples are converted by the XOR logic 57 into a register address (010).

The obtained register address is used for controlling the
30   demultiplexer 53 and the multiplexer 55, which are able to address a respective register of the register bank 54 with a received register address.

23

The multiplexer 55 retrieves the current value of the subsum S_m for the corresponding group, e.g. $S_{(010)}$ or S_2, from the register of the register bank 54 to which the

5   obtained register address is associated. This subsum S_m value is equally provided via the switch 51 to the adder 52. The adder 52 adds the determined product $r_j^0 x_j$ to the received subsum S_m.

10   The new subsum S_m is then stored again via the demultiplexer 53 into the register of the register bank 54 to which the selected register address is associated. The calculation of the subsums S_m is indicated in figure 6 as step 602.

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This procedure is performed for the current integration cycle analogously for all N input samples x_n.

After a respective integration cycle, the multiplexer 55

20   outputs the value of the subsums S_m in all registers to the combining unit 56. The combining unit 56 then combines all subsums S_m to obtain the $K+1$ correlation values C^k.

25   For the first replica code sequence, the correlation value C^0 is simply calculated as the sum of all subsums S_m:

$$C^0 = \sum_{m=0}^{2^K-1} S_m$$

30

This is indicated in figure 6 as step 603.

For the kth replica code sequence, with $k = 1,...,K$, the respective sign change in each group is taken into account. The correlation value C^k is calculated to be:

5    $$C^k = \sum_{m=0}^{2^k-1} b_{k,m} S_m ,$$

where for a respective value of m with $m = (m_1,...,m_K)$, $b_{k,m}$ is defined to be $b_{k,m} = \begin{cases} 1 & m_k = 1 \\ -1 & m_k = 0 \end{cases}$ for the kth replica code sequence $k = 1,...,K$. Thus, the respective value of b_k depends

10   again on the replica code sequence k and on the group m for which it is needed in the sum.

The calculation of the correlation values C^k for the last K replica code sequences, which corresponds to the

15   calculation of the K correlation value C^k in the first embodiment, is indicated in figure 6 as step 604.

With the two above described exemplary embodiments, it becomes apparent that it is not necessary to perform a

20   tracking correlation for each replica code sequence using all the received signal samples. It is sufficient to calculate once a subsum for various groups of received signal samples, and then to combine these subsums differently. Since the subsums can be the same for all

25   replica code sequences, a reduction of the computational load can be achieved.

It is to be understood that in the described embodiments the different replica code sequences can also be

30   different, possibly overlapping sections of a single, larger replica code sequence.

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While there have been shown and described and pointed out fundamental novel features of the invention as applied to a preferred embodiment thereof, it will be understood
5   that various omissions and substitutions and changes in the form and details of the devices and methods described may be made by those skilled in the art without departing from the spirit of the invention. For example, it is expressly intended that all compositions of those
10 elements which perform substantially the same function in substantially the same way to achieve the same results are within the scope of the invention. Moreover, it should be recognized that structures and/or elements and/or method steps shown and/or described in connection
15 with any disclosed form or embodiment of the invention may be incorporated in any other disclosed or described or suggested form or embodiment as a general matter of design choice. It is the intention, therefore, to be limited only as indicated by the scope of the claims
20 appended hereto.